

PATENT

IN THE UNITED STATES PATENT OFFICE

Applicants: Ahmad R. Ansari et al.
Assignee: Xilinx, Inc.
Title: "Method and Apparatus for Synchronized Buses"

Serial No.: 10/084,569 File Date: February 27, 2002
Examiner: Unknown Art Unit: 2185
Docket No.: X-987 US Conf. No.: 7959

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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Pursuant to 37 C.F.R. 1.56, Applicants bring to the attention of the Examiner the One Hundred Seven (107) references listed in the attached Form PTO-1449. A copy of each is enclosed herein.

These references were cited in related U.S. patent applications. This Information Disclosure Statement is being filed under 37 CFR 1.97(b) prior to the receipt of a first office action.

Citation of the above documents shall not be construed as an admission that the documents are necessarily prior art with respect to the instant invention. Citation of the above documents shall not be construed as a representation that a search has been made other than as described above. Also, the citation of the above documents shall not be construed as an admission that the information cited herein is, or is considered to be, material to patentability as defined in §1.56(b).

Respectfully submitted,

Justin Liu
Attorney for Applicants
Reg. No. 51,959

I hereby certify that this correspondence is being deposited with the United States Postal Service as **first class mail** in an envelope addressed to: Commissioner for Patents, P.O. BOX 1450, Alexandria, Virginia, 22313-1450 on January 16, 2004.

Julie Matthews
Name

Signature

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Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Substitution Form 1449A/PTO

(use as many sheets as necessary)

Sheet	1	of	7
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Complete if Known

Applicati n / Conf. N .	10/084,569 / 7959
Filing Dat	February 27, 2002
First Named Invent r	Ahmad R. Ansari
Art Unit	2185
Examiner Name	Unknown
Attorney Docket Number	X-987 US

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No.¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code (if known)			
		US- 4,758,985	07-19-88	Carter	
		US- 5,142,625	08-25-92	Nakai	
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FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T *
		Country Code ² -Number ³ -Kind Code ⁴ (if known)				
		EP 0315275 A2	10-05-89	LSI Logic		
		WO 93 25968 A1	12-23-93	Furtek		
		EP 0 905 906 A2	03-31-99	Lucent		
		EP 1 235 351 A1	08-28-02	Matsushita Electric		

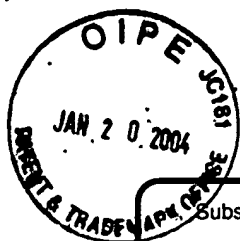
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Substitute for form 1449A/PTO		Complete if Known	
		Application / Conf. N .	10/084,569 / 7959
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Filing Dat	February 27, 2002
		First Named Invent r	Ahmad R. Arsa
		Art Unit	2185
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		Attorney Docket Number	X-987 US
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OTHER – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		SAYFE KIAEI et al., "VLSI DESIGN OF DYNAMICALLY RECONFIGURABLE ARRAY PROCESSOR-DRAP," IEEE, February 1989, pp. 2484-2488, V3.6, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		VASON P. SRINL, "FIELD PROGRAMMABLE GATE ARRAY (FPGA) IMPLEMENTATION OF DIGITAL SYSTEMS: AN ALTERNATIVE TO ASIC," IEEE, May 1991, pp. 309-314, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		G. MAKI et al., "A RECONFIGURABLE DATA PATH PROCESSOR," IEEE, August 1991, pp. 18-4.1 to 18-4.4, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		JACOB DAVIDSON, "FPGA IMPLEMENTATION OF RECONFIGURABLE MICROPROCESSOR," IEEE, March 1993, pp. 3.2.1 - 3.2.4, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
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		MICHAEL J. WIRTHLIN et al., "THE NANO PROCESSOR: A LOW RESOURCE RECONFIGURABLE PROCESSOR," IEEE, February 1994, pp. 23-30, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		WILLIAM S. CARTER, "THE FUTURE OF PROGRAMMABLE LOGIC and ITS IMPACT ON DIGITAL SYSTEM DESIGN," April 1994, IEEE, pp. 10-16, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
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		OSAMA T. ALBAHARNA, "AREA & TIME LIMITATIONS OF FPGA-BASED VIRTUAL HARDWARE," IEEE, April 1994, pp. 184 - 189, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	

Examiner Signature	Date Considered
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First Named Inventor	Ahmad R. Ansari
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Art Unit	2185
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Examiner Name	Unknown
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		Number - Kind Code (if known)			
		US- 5,473,267	12-05-95	Stansfield	
		US- 5,742,180	04-21-98	DeHon et al.	
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		US- 5,705,938	01-06-98	Kean	
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		US- 5,835,405	11-10-98	Isui et al.	

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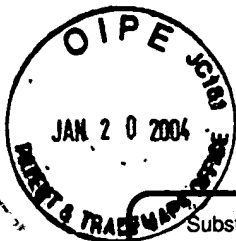
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OTHER - NON PATENT LITERATURE DOCUMENTS

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Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, pp 2-109 to 2-117, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
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		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," January 27, 1999, Ch. 3, pp 3-1 TO 3-50, Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124	
		WILLIAM B. ANDREW et al., "A FIELD PROGRAMMABLE SYSTEM CHIP WHICH COMBINES FPGA & ASIC CIRCUITRY," IEEE, May 16, 1999, pp. 183-186, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 2000, Ch. 3 pp 3-1 TO 3-117, Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124	

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		Number - Kind Code (if known)			
		US- 6,011,407	01-04-00	New	
		US- 6,172,990	01-09-01	Deb et al.	
		US- 5,970,254	10-19-99	Cooke et al.	
		US- 5,760,607	06-02-98	Leeds et al.	
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		US- 6,020,755	02-01-00	Andrews et al.	
		US- 6,279,045	08-21-01	Muthujumaraswathy et al.	<div style="text-align: center;"> RECEIVED JAN 22 2004 Technology Center 2100 </div>
		US- 6,096,091	08-01-00	Hartmann	
		US- 6,178,541	01-23-01	Joly et al.	
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